Inorganic Nanocomposite Solar Cells
by Atomic Layer Deposition (ALD)

Investigators
Stacey Bent, Professor, Department of Chemical Engineering; James Harris, Professor, Department of Electrical Engineering; Michael McGehee, Associate Professor, Department of Materials Science and Engineering; Bruce Clemens, Professor, Department of Materials Science and Engineering; Jeffrey King, David Jackrel, Post-Doctoral Researchers; Evan Pickett, Michael Rowell, Vardaan Chawla, Jonathan Bakke Graduate Researchers, Stanford University; Ben Tran, Kristine Pangan-Okimoto, Undergraduate Researchers, Stanford University

Abstract
This project is a fundamental study into the development of low-cost, thin film solar cells. It explores the fabrication of semiconductor nanocomposites for photovoltaics using nanostructured inorganic materials and atomic layer deposition (ALD). In thin film technologies, there exists a common problem with conversion efficiency due to poor materials quality: the photogenerated electrons and holes cannot travel very far before recombination (short free-carrier diffusion lengths) and are hence lost for power conversion. If the solar cell can be made using nanoscale heterojunctions, then every photogenerated carrier will have less distance to travel, and the problem of recombination can be greatly reduced. The proposed designs allow collection of all photogenerated carriers even in poor quality materials, thus making low cost deposition routes acceptable. We have performed modeling studies on single and multijunction device geometries which show that the negative effects of short minority-carrier lifetimes, namely high dark current, will be exacerbated by the large increase in junction area that occurs with nanostructuring. As a result, it appears that a good candidate for nanostructuring would be a material where low mobility—not short lifetimes—is the reason for low diffusion length. Another solution is to relax the size scale for the nanostructuring, from 100 nm to 100’s of nanometers or even a few microns. This will allow a compromise to be reached between collecting the maximum number of carriers and minimizing the interface area. Our experimental efforts have focused on an absorber material based on Cu2ZnSnS4 (CZTS), which will ultimately be incorporated into nanostructured devices. CZTS, which is comprised of earth abundant materials, has been deposited both by sputtering and chemical bath deposition (CBD) on planar substrates. Progress has been made in development of low cost methods of deposition of the semiconductor thin film, based on techniques that utilize chemical bath deposition, ion exchange, and sulfidization. Furthermore, high quality CZTS films have been made by sputter deposition combined with sulfidization, as well as by reactive sputter deposition. Nanostructured templates of both hole and pillar arrays were successfully formed on silicon using nanosphere lithography and reactive ion etching. Over the course of the project, several tools were developed to make or study the nanocomposite solar cells, including an ALD reactor, sputter deposition system, sulfidization apparatus, and a scanning probe microscope.
Introduction

This project is a fundamental study into the development of low-cost, thin film solar cells. The project explores the possibility of fabricating semiconductor nanocomposites for photovoltaics using nanostructured inorganic materials and atomic layer deposition (ALD). The ultimate goal is a photovoltaic cell built by high-throughput techniques where nanoporous structures, ultrathin layers, and multiple junctions are used to achieve good energy conversion efficiencies at low cost. This report will describe the progress that was made on several fronts, including fabrication of nanostructured templates, deposition of inorganic semiconducting materials, and development of several tools needed to make or study the nanocomposite solar cells, including an ALD reactor, sputter deposition system, sulfidization apparatus, and a scanning probe microscope.

Background

There is a strong need for the development of photovoltaic cells with low cost, high efficiency, and good stability. In thin film technologies, there exists a common problem with conversion efficiency due to poor materials quality: the photogenerated electrons and holes cannot travel very far before recombination (short free-carrier diffusion lengths) and are hence lost for power conversion. If the solar cell can be made using nanoscale heterojunctions, then every photogenerated carrier will have less distance to travel, and the problem of recombination can be greatly reduced. ALD is particularly well suited for this application since it can allow for highly uniform deposition on complex non-planar nanostructures with controllable thickness. For somewhat larger dimensions (100 nm to a few microns), other inexpensive deposition methods may also be employed. With short diffusion lengths for the photogenerated carriers, the materials constraints can be relaxed, and low cost deposition routes become acceptable.

Figure 1: Cross-sections of nanointerpenetrated p/n junction solar cell geometries, each requiring different nanofabrication; $L_d$ is the minority carrier diffusion length. A) Heterojunction geometry; nanoholes are etched into a planar p-type absorber, then the n-type window is conformally deposited by ALD or CBD. B) PIN geometry: p-type material is first nanostructured into pillars, then the intrinsic absorber and n-type window are conformally coated.

Figure 1 illustrates two proposed geometries for single junction solar cells that provide long absorption lengths and short photogenerated carrier paths. By
nanostructuring at the correct length scale, the photogenerated carrier path-lengths can be kept below the minority carrier diffusion length, greatly reducing bulk recombination.

Results

There are three major issues which must be addressed in the proposed solar cells. First is the development of the nanostructured substrates (or absorbers) with variable pore size and morphology. Second is the issue of deposition of the other material forming the p/n junction and the subsequent growth of additional layers, such as compound semiconductors, into the nanostructured substrate. The third challenge is the electrical connection and current collection from all of the nanostructured p/n junctions.

Nanostructuring - Fabrication

The nanostructured substrates (or absorbers) could potentially be fabricated by three techniques: nanosphere lithography, laser interference (or holographic) lithography, or anodization of a metal such as aluminum.[1-3] The primary reason for nanostructuring is to create a device that is optically thick to efficiently absorb the incident sunlight, and to simultaneously have every photogenerated electron-hole pair be very close to the p/n junction with respect to the minority carrier diffusion length, to minimize recombination losses. The minority carrier diffusion length in high quality silicon can be as long as 1 mm, and only a few hundred microns of material are needed to absorb over 95% of the incident light. As a result, high quality silicon devices have achieved efficiencies near their theoretical limit. With poor quality (i.e. cheaply deposited) inorganic semiconductors, the diffusion length can be on the order of only 100 nm, while the absorption length is a micron at best. This leads to poor efficiencies in planar solar cells made from these materials, since only a small fraction of the sunlight is absorbed within a minority carrier diffusion length of the p/n junction, and many of the photogenerated minority carriers recombine before reaching the junction. Nanostructuring addresses this problem, provided the pore radius of the nanostructures is on the order of the minority carrier diffusion length. Nanosphere lithography is well-established for the 100 – 500 nm length scales, and interference lithography for length scales above about 200 nm. Some preliminary studies using 100 nm and 200 nm carboxylated polystyrene nanospheres to pattern crystalline and amorphous silicon substrates have been done.

The nano-interpenetrated p-type/intrinsic/n-type (PIN) structure (Fig. 1B) is fabricated by first nanostructuring the substrate (p-type in Fig. 1) into spaced nanopillars (rather than nanoholes) and then the absorbing intrinsic layer and n-type layer are conformally deposited into the nanostructure. The intrinsic layer is kept thin enough to not planarize the structure. The n-type film above then planarizes the structures, allowing the top electrical contact to be more easily deposited. The nano-interpenetrated p-n junction (Fig. 1A) is fabricated by nanostructuring an array of spaced holes into the absorber layer. The n-type layer is then deposited conformally into the holes. In either structure, thin interface layers could be grown in between the layers to reduce recombination at the large surface area junction. [2, 4]

We have fabricated both nanopillars and nanoholes in silicon using nanosphere lithography and reactive ion etching (RIE). Close-packed arrays of both holes and pillars

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were fabricated using 200 – 500 nm diameter carboxylated polystyrene spheres. The spheres were spin coated, and RIE was performed with an Applied Materials Precision 5000 plasma etcher using standard silicon etching conditions. Ordered arrays of pillars were fabricated using polystyrene spheres as the etch mask in RIE. Arrays of holes were fabricated by first reducing the sphere diameter using an oxygen plasma etch, then depositing chromium and performing liftoff in toluene to remove the spheres. The film with chromium mask was then etched in RIE, and the holes in the metal (where the spheres had been) became etched into the silicon. Figure 2 shows SEM images of spheres spun onto silicon before (Fig. 2A) and after (Fig. 2C) diameter reduction, as well as after RIE to create both pillar (Fig. 2B) and hole arrays (Fig. 2D).

![SEM images of nanospheres (NS) and RIE etched nanostructures in silicon. A) 500 nm diameter carboxylated polystyrene NS spin-coated on silicon substrate. B) Nanopillars created by RIE from NS mask in Fig 2A. C) 200 nm NS spun onto silicon and etched in oxygen plasma to reduce their diameters to roughly 150 nm. D) Nanoholes in silicon created from NS array in Fig. 2C using chromium etch mask during RIE.](image)

**Nanostructured PV – Design Calculations**

The second major challenge is the deposition of the other material forming the p/n junction into the nanostructured substrate, and the larger concern of what solar cell materials are appropriate to nanostructure in general. A thrust of the project was focused on theoretical modeling in order to determine materials design parameters. We have performed modeling studies on single and multijunction device geometries, buffer layers, pore dimensions, and materials electrical and optical properties, such as bandgap, free-carrier mobility, free-carrier lifetime, doping density, and dielectric constant. The electrical properties have been modeled in a 1-D geometry (using the modeling program AMPS), or evaluated using models from the literature, and 2-D modeling was accomplished using Sentaurus in order to more fully investigate the effects of different nanostructure geometries and the effects of materials parameters on nanostructured devices.[4,5,6] Buffer layers that could be used to reduce the recombination at the p/n junction were 1-D modeled to evaluate different buffer layer/device materials combinations.
In terms of selecting a materials system for use in the nanostructured design, the device performance of a candidate material should be limited by the minority carrier diffusion length in planar structures, since this is the problem that nanostructuring addresses. There are many inorganic solar cell materials that have short diffusion lengths when deposited cheaply; these methods often lead to small grain polycrystalline material, or large impurity concentrations (point defects). The diffusion length, \( L_D \), can be determined from the carrier lifetime, \( \tau \), and the diffusion coefficient or the mobility, \( D \) and \( \mu \), respectively:

\[
L_D = \sqrt{D \tau} \sim \sqrt{\mu \tau}
\]  

A short effective diffusion length can be caused by either a low mobility or a low lifetime, and these two properties are not necessarily related to each other. Quite often, these short diffusion lengths are the result of recombination through traps which leads to short minority-carrier lifetimes. Unfortunately, the negative effects of short minority-carrier lifetimes, namely high dark current, will be greatly exacerbated by the large increase in junction area that occurs with nanostructuring. As a result, it appears that a good candidate for nanostructuring would be a material where low mobility—not short lifetimes—is the reason for low diffusion length, such as hydrogenated amorphous silicon (a-Si:H). Kayes, et al. pointed out in 2005 that, somewhat counter-intuitively, a material that has a high free-carrier mobility, such as crystalline silicon or GaAs, would have excessive leakage current in a nanostructured interpenetrated p/n junction geometry; this would cause the open-circuit voltage, and thus the efficiency, to drop almost to zero.\[5\] Another solution is to relax the size scale for the nanostructuring, from 100 nm to 100’s of nanometers or even a few microns. This will allow a compromise to be reached between collecting the maximum number of carriers and minimizing the junction (interface) area. We have explored this approach.

2D modeling was performed using Synopys’ Sentaurus Device Simulator, and shows a decrease in efficiency with the introduction of nanostructuring (Figures 3 and 4). A planar GaAs cell, as modeled by the software, has an efficiency of about 17%. The introduction of large microstructures – 10 \( \mu \)m n/p pillars – reduce the efficiency to 9%. A GaAs cell with 1 \( \mu \)m wide n/p pillars has an efficiency of about 8%, while 100 nm n/p pillars have a further efficiency drop to below 4%. This is consistent with predictions that nanostructuring “highly perfect” absorbers – such as crystalline semiconductors – would not yield increased efficiency. The decrease in efficiency for silicon was similar. Oddly, most of the decrease in efficiency was due to a drop in short-circuit current, not in open-circuit voltage, which requires further exploration.

In addition, as expected, increasing minority carrier lifetimes or mobilities increased cell efficiency, but planar cells were always more efficient than their structured counterparts, as shown in Figure 5. Carrier mobilities were varied from 0.01-1 times their “real” values and minority carrier lifetimes from 1 ns to 1000 ns. Figure 6 shows the high levels of recombination in such a cell.
Based upon these results, nanostructuring does not appear to present any benefit in “good,” i.e. highly perfect, absorber materials. Benefits to “bad,” i.e. highly imperfect, materials seem small as well, although more work needs to be done here. Thus, more of the parameter space must be explored, such as altering the aspect ratio of the p- and n-doped pillars to account for different minority carrier diffusion lengths. The effects of trap density – such as a high trap density in a less perfect absorber – should also be explored. More complex models, such as those accounting for doping dependent mobility and free carrier absorption, should be developed.

Figure 3. GaAs device geometry and doping parameters. Structure size was varied from 10 µm to 100 nm.

Figure 4. Si device geometry.

Figure 5. Efficiency versus lifetime multiplication factor for GaAs nanostructured cells.

Figure 6. SRH recombination rates in a nanostructured cell.

Deposition of Semiconducting Materials

For our PV studies, we chose to investigate the I$_2$-II-IV-VI$_4$ class of materials. This class can be conceptualized by starting from the I-III-VI$_2$ class (i.e. Cu$_2$InGaSe$_4$) and splitting the group III element into one group II and one group IV element to maintain an average of four valence electrons per constituent atom. There is one possible candidate material from this class, Cu$_2$ZnSnS$_4$ (CZTS), which has an attractive band gap of 1.4-1.5 eV. CZTS is a material that is comprised of abundant, non-toxic elements that has
potential application in conventional thin film as well as nanostructured photovoltaic systems. The photovoltaic materials can be deposited by ALD, chemical bath deposition and sputter deposition.[7] An ALD reactor has been built to deposit semiconductor materials (as described later in report).

We have investigated alternative methods of film deposition that lend themselves to low-cost high-throughput processing. Specifically, we have developed a wet chemical approach based on chemical bath deposition (CBD) and ion exchange. A 2 layer stack design, incorporating discrete CBD-deposited ZnS and SnS films has been developed. The resulting film is then soaked in a CuCl₂ solution, which yields incorporation of Cu into the semiconducting film via ion exchange since Cu²⁺ has higher standard reduction potentials than Zn²⁺ and Sn²⁺.[8] After deposition of this precursor film, sulfidization anneals at roughly 500-600°C are performed in a hydrogen sulfide environment to convert the layers into polycrystalline CuₓZnₓSnₓS films. Other CBD and ion exchange process flows were also investigated for forming thin films of CZTS. In addition to the CZTS based materials, we have also been investigating the CBD of CdS, which is the standard window layer for quaternary PV modules such as CIGS.

CBD is a solution-based deposition technique used for economical growth of thin films on a variety of substrates. The method is applicable for many different materials, including oxides and sulfides.[7] It is a well-established technique used commercially for growth of CdS films in both CIGS and CdTe photovoltaic modules. This technique involves the growth of films from a solution comprised of metal salts, sulfur-containing chemicals (e.g. thiourea), and various complexing agents. It is applicable to a wide range of materials, including Cu₂S, ZnS, and SnS. For example, in a relevant study, Nair et al. produced CuSnS thin films by heating SnS-CuS layers deposited by chemical bath.[9] We have successfully grown CdS, ZnS, and SnS by CBD.

For CBD growth of CdS, a substrate was immersed in a hot (60 – 100 °C), well-stirred aqueous solution containing cadmium salt, a sulfur source (e.g. thiourea), an ammonia salt, and ammonia hydroxide. For our experiments, the deposition bath was maintained at 85 °C and contained cadmium sulfate, ammonium sulfate, thiourea, ammonium hydroxide, and deionized water. Test structures of monocrystalline p-type silicon were nanostructured via nanosphere lithography, and a ~ 100 nm thick n-type CdS film was then deposited on the structure, as shown in Figure 7 below. Figure 8 shows XPS analysis of the film after a 20 second argon sputter which indicates a composition of 51% Cd, 29 % S, and 20 % O. The film contains a large amount of oxygen, likely in the form of cadmium hydroxide. ZnS was grown via several different bath compositions. The best results were found using Zn(OAc)₂ as the Zn²⁺ source; trisodium citrate and ammonium hydroxide as the complexing agents; thiourea as the sulfide source; and water as the solvent. [10] Depositions at 70 °C for 1 hour yielded films ~ 400 nm in thickness. SnS was grown using SnCl₂, acetone, triethanolamine, water, ammonium hydroxide, and thioacetamide.[12,13] Depositions at 25 °C yielded ~ 400 nm uniform, brown-orange films after 18 hours. A two layer composite structure was formed by sequential application of the SnS and ZnS bath deposition to molybdenum coated substrates. Figure
Figure 7. Cross sectional SEM image of CdS/Si nanostructured p-n junction at higher magnification.

Figure 8. XPS analysis of CdS film deposited by CBD.

Figure 9. Cross sectional SEM image of ZnS/SnS film deposited via CBD.

Figure 10. Auger depth profile analysis of ZnS/SnS film deposited via CBD.

Cu was successfully incorporated into the CBD films via ion exchange. The precursor films were soaked in an aqueous solution of CuCl₂ for times ranging from minutes to several hours and the resulting films were analyzed using Auger depth profiling. A representative profile is shown in figure 11, which shows data for a 2 hour ion exchange. The data shows that copper was successfully incorporated into the film, with Zn and Sn still present. The profile shows that the film is Cu-rich near the surface, but significant copper has been incorporated throughout the film.
Post-deposition sulfidization heat treatments were performed on CBD-deposited and ion exchanged films. The sulfidization chamber is described in more detail in the next section of the report. Exposure of precursor films to a H$_2$S environment for 2 hours at 500° C facilitated removal of oxygen and interdiffusion of the precursor layers, resulting in a uniform composition. An SEM image of the film surface is shown in Figure 12 and the resulting Auger depth profile is shown in Figure 13. The sample showed a remarkably uniform composition, but is Zn rich (Cu:Zn:Sn:S = 2:2:1:4 instead of 2:1:1:4).

The absorbance of the films at different processing stages has been studied using transmission and diffuse reflectance. Figure 14 shows absorbance characteristics of a bath deposited SnS film, indicating a band gap at $\sim$ 1.9 eV. Figure 15 shows absorbance characteristics of a sulfidized precursor film (CZTS), indicating a band gap at 1.46 eV, which is the predicted band gap position for Cu$_2$ZnSnS$_4$. 

**Figure 11:** Scanning Auger depth profile, copper ion exchanged ZnS/SnS CBD film.

**Figure 12.** SEM image of CZTS film surface after 2 hour H$_2$S heat treatment.

**Figure 13.** Scanning Auger depth profile of CZTS film after 2 hour H$_2$S heat treatment.
We have also deposited films of CZTS onto (100) silicon substrates and molybdenum coated glass substrates using two different sputtering processes. Metal films were grown at the correct stoichiometry and then annealed in an H2S atmosphere at temperatures ranging from 400-550°C to incorporate sulfur into the film and create the CZTS phase. X-ray photoelectron spectroscopy (Figure 16) was used to confirm the presence of copper, zinc, tin and sulfur and to establish homogeneity in the film by depth profiling (Figure 17). The films show the correct stoichiometry and have homogenous composition. X-ray diffraction was used to confirm that the correct CZTS phase was formed during the anneal (Figure 18). We used high intensity synchrotron radiation to resolve the smaller CZTS peaks and differentiate them from ZnS peaks.
After characterization, these films were incorporated into device stacks seen in Figure 19. The Mo was grown by sputtering, the CdS by bath deposition and the ZnO:Al was grown by reactive DC sputtering. The current-voltage (IV) characteristics of the devices were tested using the AM1.5 spectrum (Figure 20). The IV curve shows that electron-hole pairs are being generated in the absorber and extracted from the device. However, the devices have very low shunt resistance which is detrimental to the fill factor and device efficiency. This can be explained by pinholes in the film created during the H₂S anneal that is required to incorporate sulfur into the film.

In an effort to eliminate the defects created during the H₂S anneal, we have also grown CZTS films using a reactive sputtering process. H₂S is introduced into the sputtering ambient during the metal deposition and becomes incorporated into the growing film. While this process is still under development, it has shown some promising results. A comparison of the reactively sputtered (RS) films and H₂S annealed (HA) films shows that the RS films are textured in the [112] direction and are of significantly better...
quality than the HA films (Figure 21). The high quality of the films can also be seen in the SEM image (Figure 22) of a film cross section.

![Figure 21: XRD patterns of CZTS films deposited by sputter deposition plus sulfidization vs reactive sputter deposition](image)

![Figure 22: Cross sectional SEM image of CZTS film deposited by reactive sputter deposition](image)

These films were also incorporated into the same device stacks as the HA films. IV curves (Figure 23) of these devices show that they form diodes and do not have the shunt resistance problems associated with previously grown HA films. There is also an increase in current when the films are placed under illumination which points to generation of photocarriers in the CZTS film absorber. Unfortunately, no power is generated in the device because the carriers generated are recombining before they can be removed from the film. We believe this is due to cadmium penetration into the CZTS film which can be seen in the Auger depth profile in Figure 24. The mechanism for cadmium penetration it unclear at this time and future work should focus on adjusting the CdS bath deposition process to be compatible with the CZTS films.

![Figure 23: Current-voltage curves of CZTS films deposited by reactive sputtering](image)

![Figure 24: Auger depth profiles for CdS/CZTS/Mo stacks](image)
**Apparatus for depositing and testing nanocomposite PV materials**

**ALD reactor**

Construction of a new ALD reactor was completed; the reactor is shown in Figure 25. The reactor is a cold wall configuration with the ability to dose four precursors and the capacity for at least four more precursors, giving a large degree of flexibility in materials choice. The dosing of each precursor is controlled by Swagelok ALD pneumatic valves. One precursor line contains “thermal” valves which allow for the dosing of low vapor pressure materials that must be heated to high temperatures. The carrier gas is nitrogen, and its flow rate for each precursor is moderated by a mass flow controller. The sample stage is radiatively heated and capable of reaching temperatures >500 °C. The reactor is operated by a LabVIEW VI which is under testing and will have the capability to set and to monitor reactor temperature at 12 zones, to monitor the pressure inside the reactor, and to set the flow rate of the carrier gas for each precursor.

**Sputter deposition system**

In order to prepare samples of new materials such as CZTS, we constructed a five target sputtering system (Figure 26). The system consists of a load lock for rapid sample loading/unloading, a large chamber with three sputter guns for co-deposition of copper, zinc and tin, and a secondary chamber for deposition of chromium and molybdenum to be used as back contacts for CZTS devices. It includes a substrate heater for temperature control from room temperature up to 700 °C and a rate monitor to control deposition rate. We also added a H2S gas source in an attempt to incorporate sulfur into the films during the deposition process. By introducing controlled quantities of H2S into the sputtering ambient we can reactively sputter a CZTS film with the required crystal structure in a one-step process.

![Figure 25. ALD Reactor](image1)

![Figure 26. Sputter Deposition System](image2)

**Sulfidization**

A sulfidization reactor has been constructed for heat treatment of both CBD and sputtered precursor films. The apparatus is a medium vacuum (~ 5 mTorr base pressure) tube furnace based system capable of reaching temperatures in excess of 600 °C. The reactor is evacuated using a rotary vane pump, which allows a base pressure of 10 mTorr. A mass flow controller is used to control the flow of inert gas (nitrogen) in the reactor.
During sulfidization heat treatments, the vacuum line is closed, and hydrogen sulfide gas is introduced into the reactor, bringing the pressure up to ~400 mTorr in a batch style, or static condition. Periodically, the reactor can be evacuated, and the H₂S refreshed.

**Scanning Probe Microscopy**

We have developed techniques for performing various scanned probe electrical measurements on inorganic materials as an addition to our characterization techniques. Scanning probe microscopy (SPM) has become an essential tool in the last 10 years in the understanding of thin film solar cells, in particular the and CIGS (Cu(In₉Gaₓ₋₁)(S,Se)) and CdTe systems. SPM allows the direct mapping—both topographical and cross sectional—of properties such as work function, location of built-in potentials and depletion zones, and photovoltage. This technique will be particularly crucial for nanostructured solar cells in that the three-dimensional, multi-interface nature of the device makes traditional methods of characterizing the electrical junction properties, such as capacitance-voltage profiling, difficult or impossible to use. For example, for the device in Figure 1B, electrostatic force microscopy (EFM), which can measure the local work function and any variations in it due to electric fields from space charge, is the only way to observe the shape of the depletion region. This will be critical for optimizing the device structure, doping levels, and understanding the effect of any interface modifiers.

![Figure 27. Electrostatic Force Microscopy](image)
Figure 27. Electrostatic Force Microscopy of a test structure consisting of electrodes deposited on a silicon wafer with 300 nm of oxide. A topography image (a) and surface potential (b) of the red square in (c) demonstrates the high spatial and electrical resolution of this imaging mode. d) A cross section cut along the red line in (b) shows that the 100 mV applied potential difference is accurately read by the EFM to within 5%.
We successfully modified an atomic force microscope for performing EFM, which enables us to map surface potential over large areas with unprecedented resolution (see Figure 27). The standard method of mapping surface potential has been Scanning Kelvin Probe Microscopy (SKPM). EFM is a significant advancement over SKPM because it relies on the force gradient of the electrical interaction between the probe tip and the sample and not the force itself as with SKPM. This avoids the convolution of signal from the long cantilever and localizes the interaction volume to the very apex of the tip, which enables quantitative potential measurements with high spatial resolution. This is an essential advancement for investigating nanostructured devices where the device dimensions are on the length scale of the probe tip itself.

**Electrical Connection and Current Collection**

A significant challenge in the nanostructured design is the electrical connection and current collection from all of the nanostructured p/n junctions. The electrical connection will be made much simpler if the device structures can be planarized, either during or after growth. However, if the surface roughness is too great and standard metal evaporation is not sufficient to create a good electrical contact then alternative contact deposition techniques, such as screen-printing, will be investigated.

One of the biggest fundamental electrical challenges facing interpenetrated p/n junction nanostructured solar cells is the recombination at the p/n junction interface. Recombination scales linearly with the junction area, and in these cells the junction area can be orders of magnitude larger than a planar design with the same solar cross-section. There has been some work done depositing thin buffer layers (~10 nm) in between the p- and n-type materials in nanostructured cells to suppress interfacial recombination.[14,15] We performed 1-D modeling to evaluate the effects of different buffer layer/device materials combinations. It has been suggested that a buffer layer with appropriate conduction and valence band energies could reduce interfacial recombination by reducing free-carrier concentrations at the interface between the n- and p-type materials. This will increase the open-circuit voltage, but our modeling shows it comes at the cost of the device current; the lower carrier concentrations near the junction interface also reduce the electric field strength which is needed to collect the photogenerated carriers. We have therefore determined that much of the benefit of buffer layers observed in nanostructured interpenetrated p/n junction solar cells is likely the result of improved interface chemistry (passivation) at the junction, rather than an altering of electron and hole concentrations through band-level engineering.

**Conclusions**

We made progress toward development of potential nanostructured architectures and materials systems where these designs would offer significant efficiency enhancement in modules deposited using low-cost methods. It is anticipated that these architectures will yield decreased cost per watt in PV modules, allowing for a shift in global energy generation toward clean, renewable carbon-free technologies. The current world record power conversion efficiency for single-junction hydrogenated amorphous silicon solar cells is just below 10%.[16] Our device modeling showed that if nanostructuring enabled the cells to achieve 100% quantum efficiency, then the current could be increased from
16 mA/cm² up to 21.5 mA/cm², significantly increasing the open-circuit voltage as well, yielding a power conversion efficiency as high as 15%. We have also identified Cu₂ZnSnS₄ as a good test case for nanostructuring. We made films of CZTS both by sputtering and chemical bath deposition, and made photovoltaic devices for testing. Current state of the art planar cells allow efficiencies of ~5%, but it is anticipated that CIGS-like efficiencies close to 20% should eventually be possible. Nanostructuring should allow attainment of this goal with lower demand on materials quality. These devices would be single-junction cells, manufactured largely with techniques amenable to high throughput processing. This approach allows us, therefore, to move towards the design and fabrication of a nanostructured solar cell that could be made using low-cost production techniques at efficiencies matching current thin-film devices, success of which would allow reduced dependence on fossil fuel energy production worldwide.

Publications


References

Contacts
Stacey Bent, sbent@stanford.edu
James Harris, harris@snowmass.stanford.edu
Michael McGehee, mmcgehee@stanford.edu
Bruce Clemens, bmc@stanford.edu